Texas Instruments

Low Voltage Logic Families

Application Report

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Low Voltage Logic Families

This report concerns the new families of logic integrated circuits designed for a supply voltage of 3.3V, and having the suffixes LV, LVC, ALVC and LVT. The new technology of these circuits is first presented and explained; this is followed by a description of their electrical behavior under both DC and AC conditions.

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1. Introduction

At the beginning of the sixties TTL logic became established as the preferred technology for digital signal processing. Since the breakdown voltage of the multi-emitter inputs used at that time was about 5.5V, the decision was taken to use a 5V supply voltage. Since then 5V has become the standard for supply voltages with digital components.

In the meantime a number of different requirements has resulted in the need for a reduced supply voltage:

The reduction of the horizontal and vertical structure widths of modern semiconductors has now reached the stage that lower voltages are being required, because otherwise the reliability of the components would be compromised. In particular, the high field strength with 5V operation represents an increase of stress which can lead to the breakdown of the gate oxide. The result is a short circuit of the CMOS transistor which would make the component useless.

The demand for a further reduction in power consumption comes mostly from manufacturers of battery operated equipment. The power consumption results principally from capacitive loads, from the operating frequency, and from the supply voltage. Whereas the capacitance of the load and the operating frequency have a linear effect on power consumption, the consumption depends on the square of the supply voltage.

A lower power consumption however also reduces the generation of heat in subassemblies, and so can obviate the need for cooling fans, and also simultaneously improve the reliability of the components. Lower temperatures also allow an increase in the density of integration of components. For this reason, many DRAM's operate these days internally with 3.3V, and their input and output signal levels are simply made to be compatible with their external 5V environment.

	'AC11245		**'HC245**	
	V_{CC}=5.0V	V_{CC}=3.3V	V_{CC}=4.5V	V_{CC}=2.0V
t_{PLH} TYP A B / B A	4.8ns	6.5ns	15ns	40ns
t_{PLH} MAX A B / B A	9.5ns	12.5ns	26ns	130ns
V_{OH} specified up to	-24mA	-4mA	-6mA	-20µA
V_{OL} specified up to	24mA	12mA	6mA	20µA

Table 1: Changes of various parameters with the logic families HC and AC, when the supply voltage is reduced.

The logic families HC and AC can already be operated with a supply voltage of much less than 5V. With the HC family, the supply voltage is specified down to 2V in the data book; with the AC, down to 3V. The longer delay time and the reduced drive capability are however disadvantages of using a lower supply voltage which must be taken into account. Table 1 shows several examples from the data book. In order to achieve a high speed and high drive power despite a low supply voltage, it was necessary to develop new logic families.

2. Technology

The components in the logic families LV, LVC, ALVC and LVT were developed for a typical supply voltage of 3.3V. All four families have, however, functions corresponding to those in the families with 5V supply voltage (Table 2), whereby their internal circuit structures and electrical characteristics conform basically to those of their 5V "relations".

	LV	LVC	ALVC	LVT
Corresponding family with 5V supply voltage	HC	AC	AC	BCT and ABT
Process	CMOS 2.0 µm	CMOS 0.8 µm	CMOS 0.6 µm	BiCMOS 0.8 µm
Minimum supply voltage to ensure correct operation	2V	2.7V	2.7V	2.7V
Power on Demand	Not needed	Not needed	Not needed	✔
Bus Hold		All Widebus™	✔	✔
Power-Up Tristate				All LVTZ
Inputs TTL-compatible	✔	✔	✔	✔
Outputs TTL-compatible	✔	✔	✔	✔

Table 2: Characteristics of the families LV, LVC, ALVC and LVT

The families LV, LVC and ALVC use pure CMOS processes, and show the typical characteristics of CMOS circuits. LVT is based on the BiCMOS process technology. The input circuit and internal logic is implemented with CMOS components, and the output stage with bipolar transistors. As a result of this BiCMOS technology, the characteristics of CMOS (low static power consumption) are combined with those of bipolar technology (namely, high drive power, improved dynamic power consumption and the highest speed).

2.1 Power-on-Demand

A BiCMOS circuit, such as the LVT, has the highest power consumption when the output is in the 'L' state. The supply current is then mainly required in order to supply the Pull-Down transistor with base current. In order to reduce this current still further with battery-powered equipment, the "Power On Demand" (POD) circuit has been developed. This measures the current flowing in the output and then supplies the necessary base current (Figure 1). As a result of this, the supply current of the circuit I_{CCL}, and consequently the power consumption, are drastically reduced at lower frequencies (Figure 2).

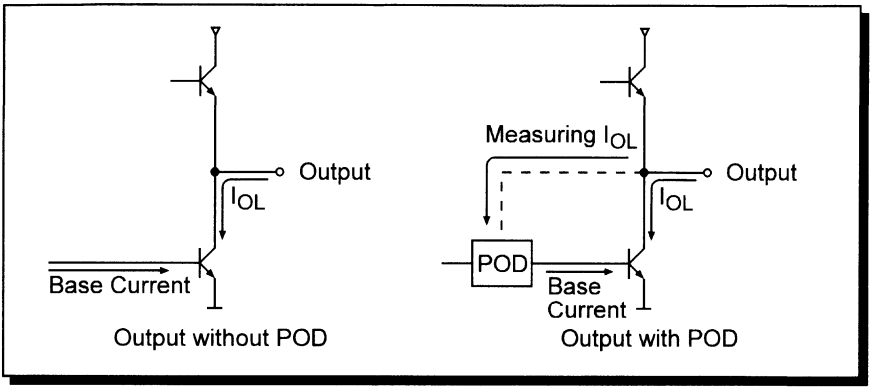

Figure 1: Output without and with Power on Demand (POD).

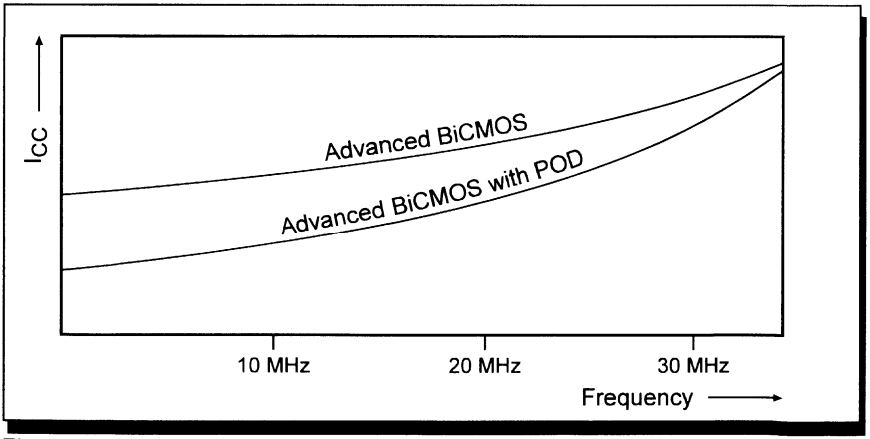

Figure 2: Increase of the supply current with increasing frequency, with and without the Power on Demand (POD) circuit.

2.2 Bus Hold Circuit

With fast circuits having CMOS inputs, an open input or a very slowly changing edge can cause oscillation of the component. With this oscillation the power dissipation of the component increases significantly, and this can result in destruction.

For this reason bus lines must always be held at a defined logic level. This is no problem with unidirectional lines, since the driver always supplies all inputs connected to it with a valid logic level. If however with bidirectional bus lines all drivers are in a high impedance state, then a voltage level will be established which is determined by the leakage currents of the components which are connected. In this situation a defined logic level can no longer be assumed. The inputs connected to this bus line now behave as open circuit inputs, and in the worst case a destruction of the component may result.

If it is not possible to keep an inactive state of the bus short enough that, during this period, no damaging voltages can build up, then it is usual to seek help with "pull-up" resistors or with split-resistor bus terminations, each consisting of a resistor connected to V_{CC} and GND. However, these resistors increase significantly both the loading of the outputs and the current drain of the complete system.

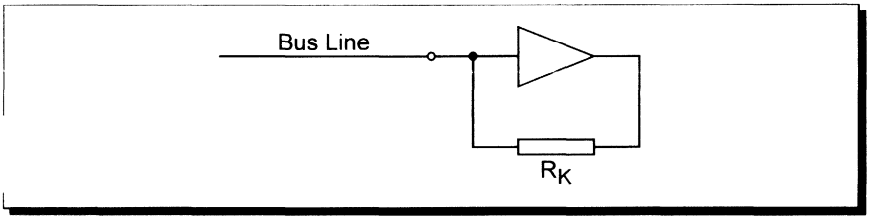

Figure 3: Bus Hold Circuit

A more elegant method of supplying inactive bus lines with a defined level is to make use of a so-called "Bus Hold Circuit" (Figure 3). In this circuit, the output of a non-inverting driver is connected back to the input with a resistor. In this way a bistable circuit ("LATCH") results, which is connected to the bus line. This circuit always holds the bus line during an inactive phase in the previous logic state. With an appropriate choice of the feedback resistor an extremely low loading of the bus line results, and a possible charge transfer of the bus line when entering the inactive state can also be avoided. The characteristics of a Bus Hold Circuit are shown in Figure 4. A detailed discussion of the Bus Hold Circuit can be found in the Application Report EB 209 from TEXAS INSTRUMENTS.

In order to reduce the necessary component count, TEXAS INSTRUMENTS has integrated the Bus Hold Circuit into the inputs of the LVC-Widebus™, ALVC and LVT families.

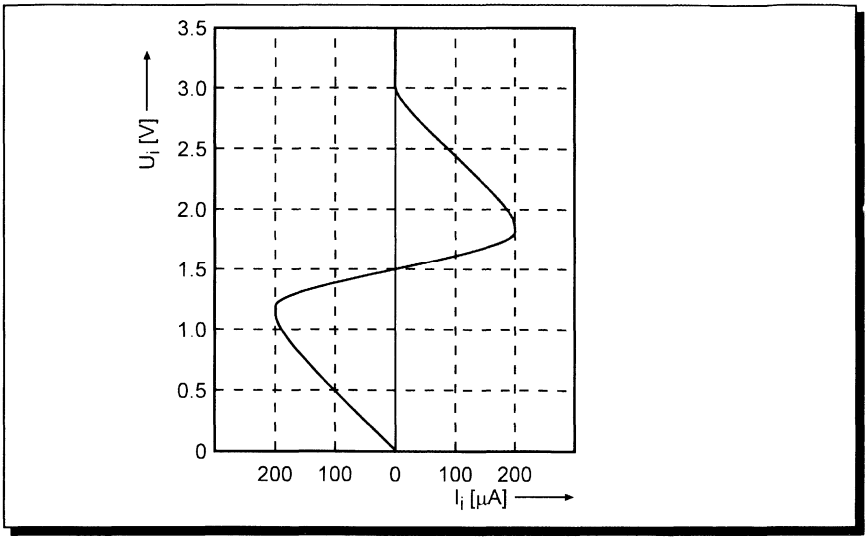

Figure 4: Input characteristics of a Bus Hold Circuit

2.3 Power-Up Tristate

If in an electronic system it is necessary to switch off the supply voltage to individual subsystems, whilst the complete system continues to operate normally, then the following circuit properties are necessary:

The inputs and outputs of all circuits which are connected to a bus and switched off must be at a high impedance, if the supply voltage is 0V.

If the supply voltage goes below the value necessary to ensure correct operation of the component, then the output must be at a high impedance. This is necessary in order not to interfere with the active part of the system during the time while switching off or on takes place.

All purely bipolar outputs with NPN transistors fulfill the requirement of being at a high impedance when the supply voltage is switched off, since a bipolar transistor is only at a low impedance when a base current is flowing, or a diode path is connected in a forward direction. A supply voltage of 0V can however no longer supply a base current, and with a NPN pull-up transistor all diode paths are blocked. Also, since the breakdown voltages of these diodes will not be reached with TTL signals, these outputs will be at a high impedance.

Additional steps must be taken in order to fulfill the second requirement of a defined switch-off behavior. With the LVTZ components a special circuit (Power-Up Tristate) has been incorporated which controls the supply voltage. If the

supply voltage falls below about 1.8V, then the output stages will be at a high impedance. In this way a defined switch-off and switch-on behavior is assured.

2.4 CMOS Pull-Up

A bipolar TTL output stage, as shown in Figure 5, has the property that, with a 5V supply voltage in the HIGH state, an output voltage of a maximum of

$$V_{CC} - (2 \times V_{BE}) = 5V - (2 \times 0.7V) = 3.6V$$

can be reached. If an output stage of this kind is used with a 3.3V supply voltage, then the maximum possible level is

$$V_{CC} - (2 \times V_{BE}) = 3.3V - (2 \times 0.7V) = 1.9V$$

Since no TTL compatible output level can be attained with V_{oh} = 1.9V, in the LVT family an additional CMOS pull-up transistor has been incorporated in parallel (Figure 5). This transistor allows an output voltage of almost V_{CC}, whilst the bipolar transistor takes over the high currents during the switching process. In this way, the bipolar output stage shows 'RAIL-TO-RAIL' switching behavior, and is compatible with the logic levels of the 5V TTL families and the 3.3V CMOS components.

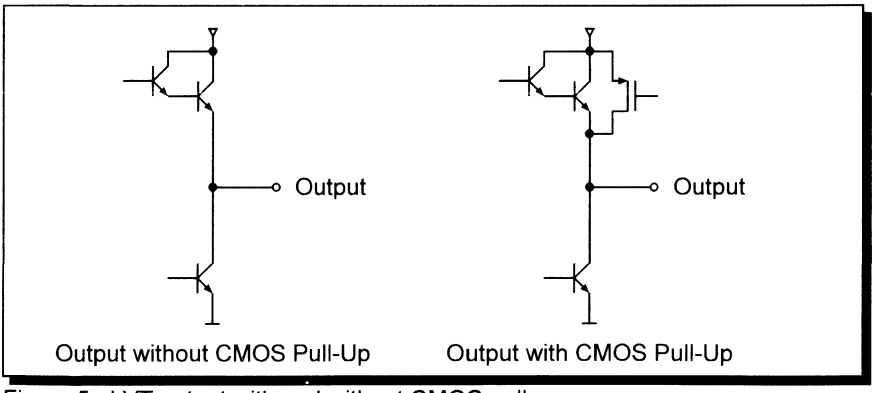

Figure 5: LVT output with and without CMOS pull-up

The newer generation of bipolar output stages (ABT and LVT) are also supplied with an auxiliary CMOS transistor parallel to the bipolar pull-down transistor. The reason for this is not to extend the voltage swing, but to improve the switching performance, mostly with respect to switching speed.

2.5 ESD Protection Circuits at the Inputs and Outputs

2.5.1 LV Family

As a protection against electrostatic discharge (ESD = ELECTROSTATIC DISCHARGE) the circuits in the LV family from TEXAS INSTRUMENTS are provided with protective circuitry at the inputs and outputs (Figure 6):

The inputs are protected against positive overvoltages by a diode to V_{CC}; two NPN transistors provide protection against negative overvoltages. An additional resistor at the input limits the input current.

The protection of the outputs against positive and negative overvoltages is provided by two diodes, one connected to V_{CC} and one to GND.

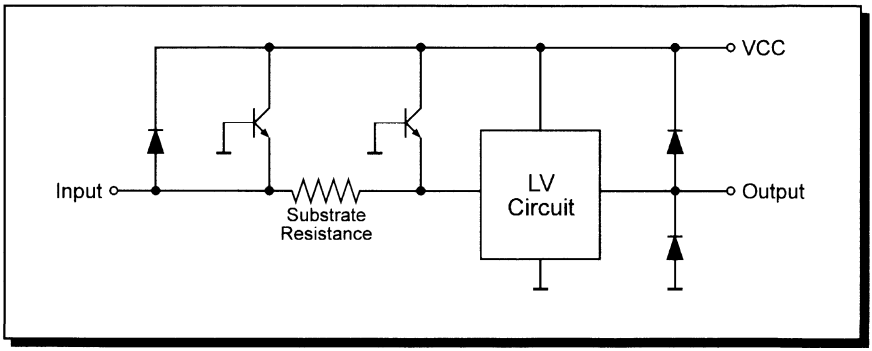

Figure 6: ESD protection circuitry in LV circuits

2.5.2 LVC Family

With LVC components the following precautions have been taken to provide protection of the circuits against electrostatic discharge (ESD = ELECTROSTATIC DISCHARGE) - see Figure 7:

The protection of the CMOS inputs against positive overvoltages is provided by two Zener diodes (Z-Diode) connected back-to-back in series. Negative overvoltages are limited by a Z-Diode and also by Z-Diodes connected back-to-back in series.

The protection of the outputs against positive and negative overvoltages is assured by a diode to V_{CC} and a Z-Diode to GND.

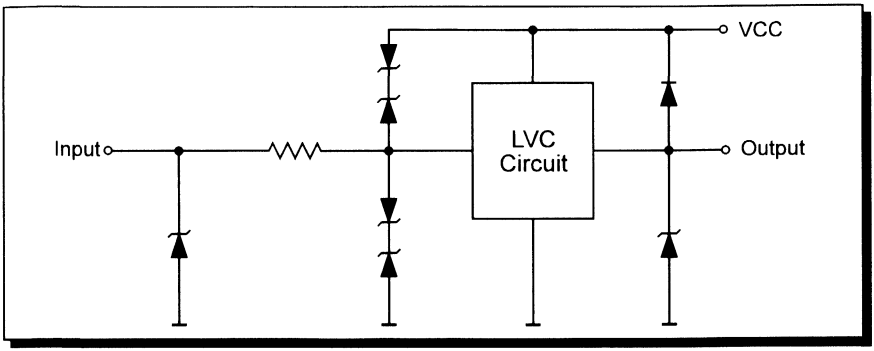

Figure 7: ESD protection circuitry in LVC circuits

2.5.3 ALVC Family

The ESD protection circuitry of the ALVC family is much the same as that of the LVC family (Figure 8):

The protection of the CMOS inputs against positive overvoltages is undertaken by a Z-Diode and two back-to-back Z-Diodes in series. Negative overvoltages are limited by a Z-Diode, and also by back-to-back Z-Diodes in series.

The protection of the outputs against positive and negative overvoltages is provided by a diode to V_{CC} and a Z-Diode to GND.

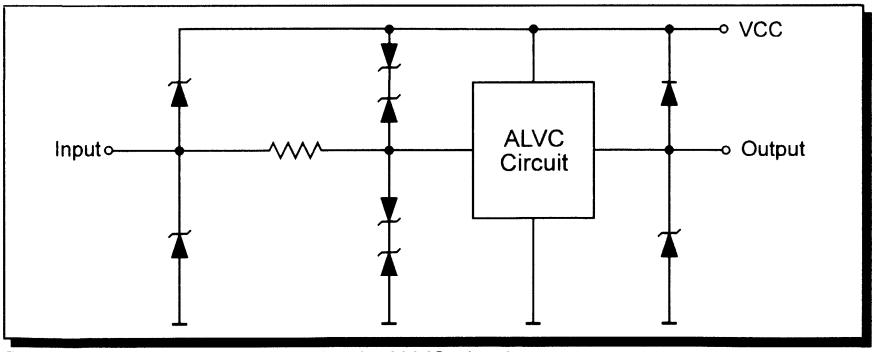

Figure 8: ESD protection circuitry in ALVC circuits

2.5.4 LVT Family

LVT components are protected against electrostatic discharge (ESD = ELECTROSTATIC DISCHARGE) with the following circuitry (Figure 9):

The protection of the CMOS inputs is provided by two NPN transistors. An additional resistor at the input limits the input current.

ESD protection is not necessary for the high-power transistors in the bipolar output stage.

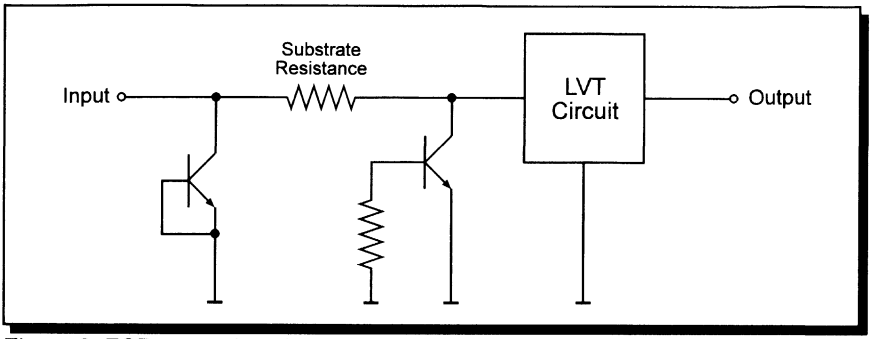

Figure 9: ESD protection circuitry in LVT circuits

3. Electrical Behavior

The electrical characteristics of the families LV, LVC, ALVC and LVT are basically similar to those of their 5V "relations" (Table 3).

	LV	LVC	ALVC	LVT
Supply Voltage	2.7V..3.6V	2.7V..3.6V	2.7V..3.6V	2.7V..3.6V
Threshold Voltage at the input	V_{CC} / 2 typ. = 1.65V	V_{CC} / 2 typ. = 1.65V	V_{CC} / 2 typ. = 1.65V	1.4V
Output Voltage	$V_{OH} = V_{CC}$ V_{OL} = 0V	$V_{OH} = V_{CC}$ V_{OL} = 0V	$V_{OH} = V_{CC}$ V_{OL} = 0V	$V_{OH} = V_{CC}$ V_{OL} = 0V
Output Current	I_{OH} = -8mA I_{OL} = 8mA	I_{OH} = -24mA I_{OL} = 24mA	I_{OH} = -24mA I_{OL} = 24mA	I_{OH} = -32mA I_{OL} = 64mA
Power on Demand	Not Needed	Not Needed	Not Needed	✔
Bus Hold		All Widebus™	✔	✔
Power-Up Tristate				All LVTZ
Static current consumption	I_{CC} = 20µA	I_{CC} = 20µA	I_{CC} = 40µA	$I_{CCH/Z}$ = 100µA I_{CCL} = 12mA
Typical delay time	9.0ns	4.0ns	2.2ns	2.4ns
Maximum delay time	18.0ns	7.0ns	4.0ns	4.0ns

Table 3: Typical electrical characteristics of a Bus Driver

3.1 Inputs and Outputs

3.1.1 Switching Threshold

Whereas the LV, LVC and ALVC families (being pure CMOS) show the voltage levels which are typical for CMOS, the LVT has been designed as a BiCMOS family with TTL-compatible voltage levels. Figure 10 shows the definitions of the input and output levels together with the typical switching thresholds of the inputs.

Table 4 explains which logic families are suitable for driving the inputs of which other families.

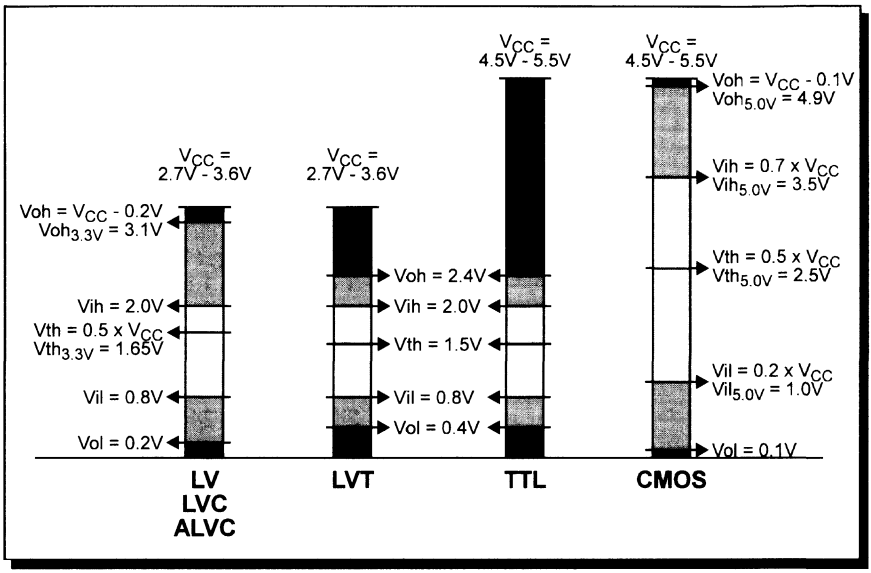

Figure 10: Definition of the voltage level for inputs (V_{il}, V_{ih}), outputs (V_{ol}, V_{oh}) and the switching threshold (V_{th}), of the families LV, LVC, ALVC, LVT, in comparison with TTL-compatible and 5V CMOS families.

		Input					
		LV	LVC	ALVC	LVT	TTL	CMOS
Output	LV	✔	✔	✔	✔	✔	
	LVC	✔	✔	✔	✔	✔	
	ALVC	✔	✔	✔	✔	✔	
	LVT	✔	✔	✔	✔	✔	
	TTL	✔	✔	✔	✔	✔	
	CMOS		✔		✔	✔	✔

Table 4: Compatibility of the inputs and outputs of the logic families LV, LVC, ALVC, LVT, in comparison with TTL-compatible and 5V CMOS families.

3.1.2 Connection to 5V CMOS

The connection of the LOW VOLTAGE families to 5V CMOS circuits is only possible in one direction: that is, 5V CMOS outputs can drive LVC and LVT inputs, but none of the LOW VOLTAGE families is able to supply the necessary voltage level for 5V CMOS inputs. For this reason the SN74ALVC164245 was developed: this is a special component for use as an interface between LOW VOLTAGE families and 5V CMOS circuits.

3.1.3 Characteristics of the Inputs Vi/Ii

The inputs of the LV (Figure 11) and ALVC circuits (Figure 13) show the same behavior as circuits of the HC family and are influenced by the two diode paths connected to GND and V_{CC} (Figures 6 and 8). Accordingly, with input voltages which are negative or beyond V_{CC}, diode characteristics can be observed (Figure 11).

The diode characteristics of the ESD protection circuitry determine the input characteristics with negative voltages of the LVC (Figure 12) and LVT families (Figure 14). The characteristics of the ALVC and LVT with positive voltages in the range from 0V to 3V are determined by those of the Bus Hold Circuit.

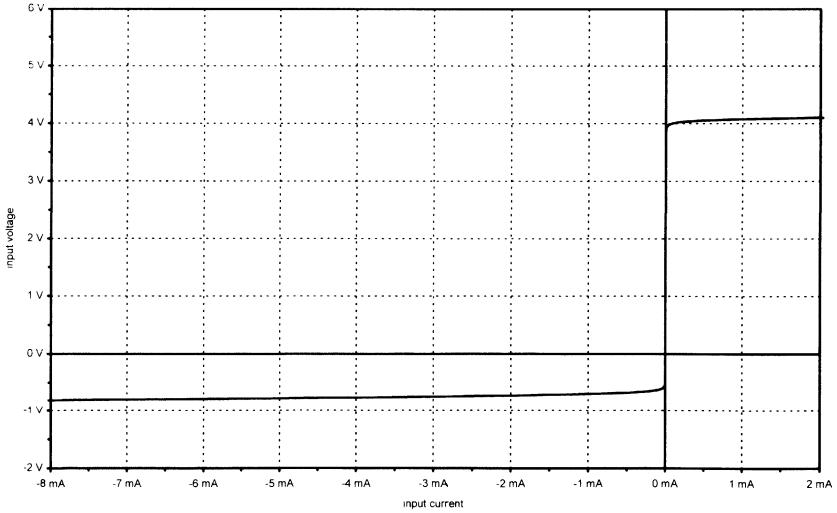

Figure 11: Input Characteristics of the SN74LV244

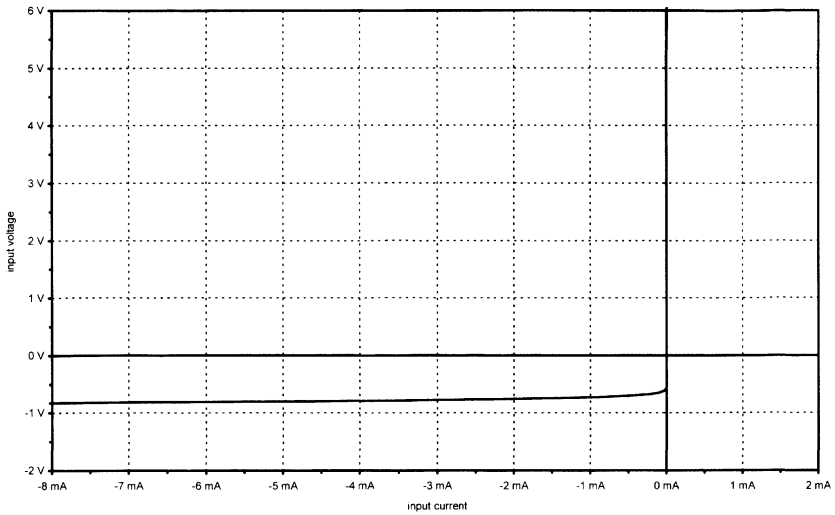

Figure 12: Input Characteristics of the SN74LVC244

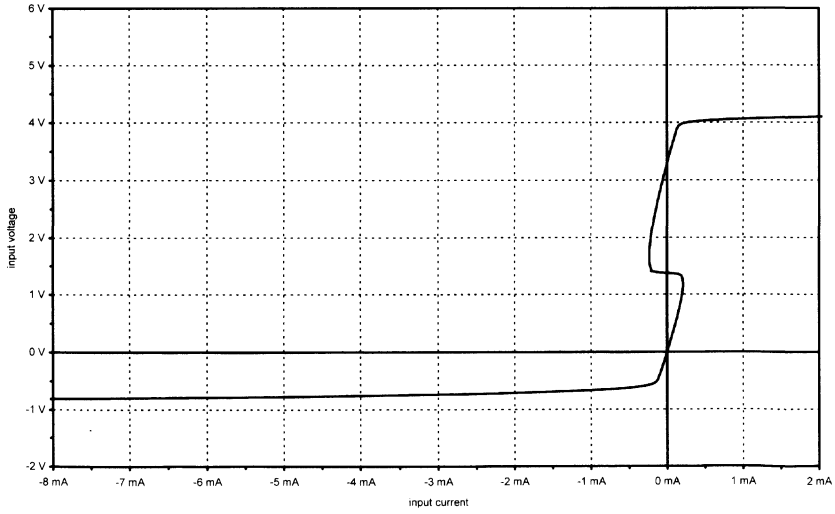

Figure 13: Input Characteristics of the SN74ALVC16244

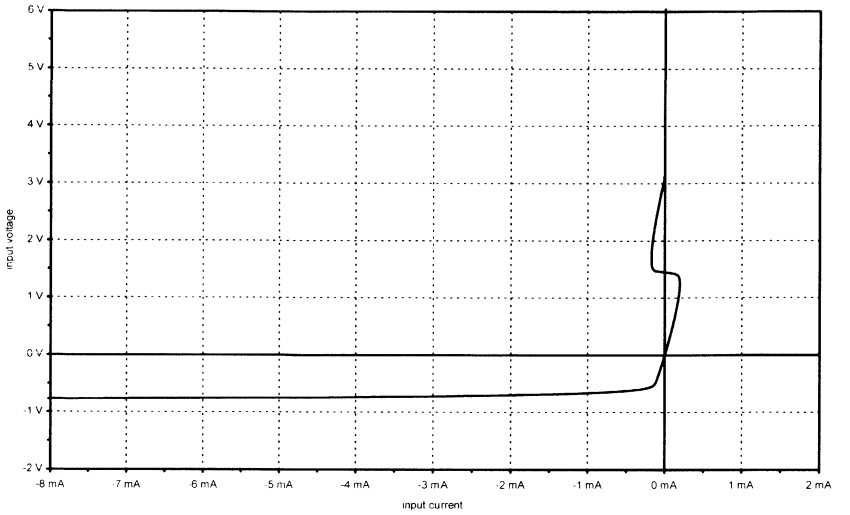

Figure 14: Input Characteristics of the SN74LVT244

3.1.4 Characteristics of the Outputs V_O/I_O

Figures 15, 16, 17 and 18 show the output characteristic curves for L and H voltage levels. These measurements were made with a load current from -200mA to +200mA, although this range can only be covered with special measurement techniques. In normal operation the maximum load currents specified in data sheets apply; however, in dynamic operation such high currents can flow for short periods whilst switching. These short current peaks do not however damage the component.

The typical characteristics of CMOS output transistors can be clearly observed at the outputs of the LV and LVC families: a straight-line resistor characteristic changes with increasing voltage drop into that of a constant current source. The bipolar output of the LVT at H level above -80mA also shows the typical CMOS characteristics resulting from the CMOS pull-up transistor (see Chapter 2.4). At currents below -80mA and at L level, the characteristics of a bipolar transistor can be seen.

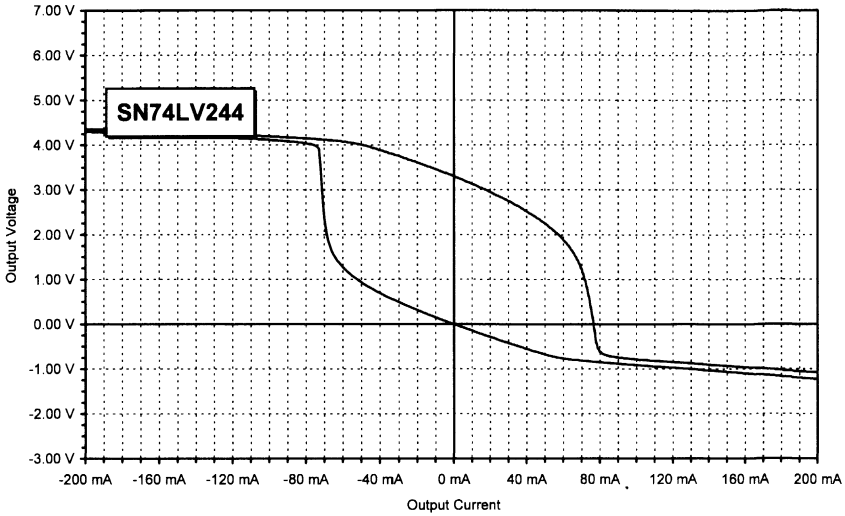

Figure 15: Output Characteristics of the SN74LV244

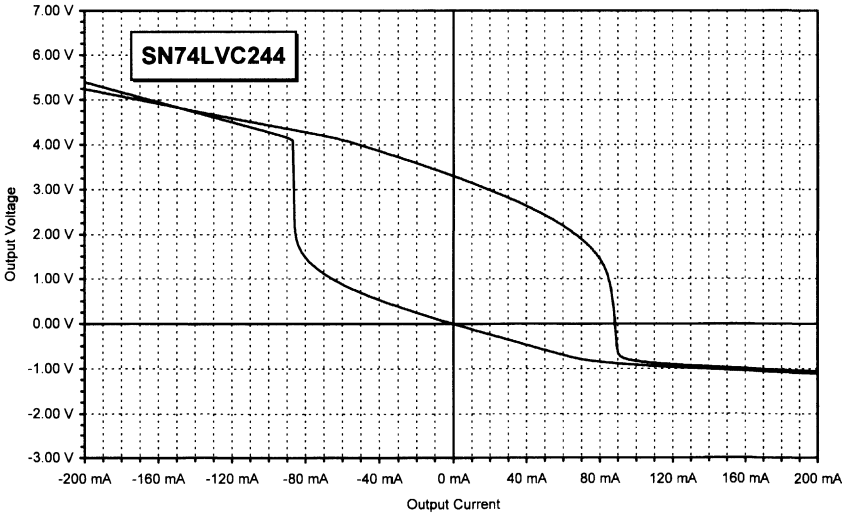

Figure 16 Output Characteristics of the SN74LVC244

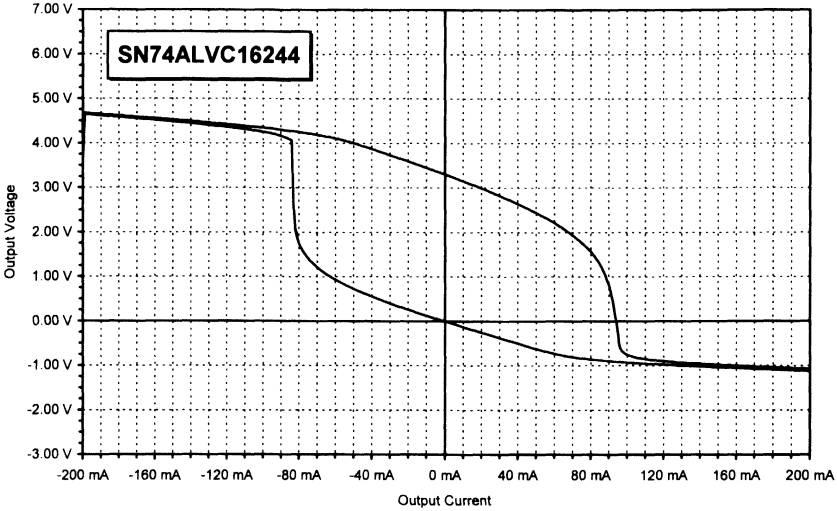

Figure 17: Output Characteristics of the SN74ALVC16244

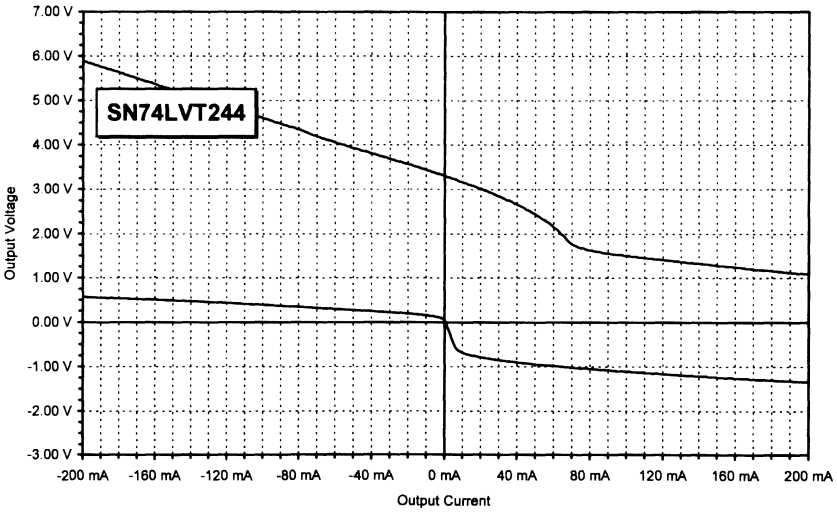

Figure 18: Output Characteristics of the SN74LVT244

3.2 No Supply Voltage

In systems where the supply voltage is sometimes switched off, the behavior of the component at V_{CC} = 0V is of interest. The four circuit families show significantly different behavior in this respect.

3.2.1 LV without Supply Voltage

The ESD protection circuitry used with LV circuits (Figure 6, Page 10) has the result that the voltages at the inputs and outputs never can be higher than one diode forward voltage drop above the voltage of the supply. With a supply voltage of 0V it is therefore not possible to apply a voltage of more than about 0.7V to the inputs and outputs, without thereby damaging the component (Figures 19 and 20). LV circuits are therefore not suitable fur use in systems where the supply voltage is sometimes switched off.

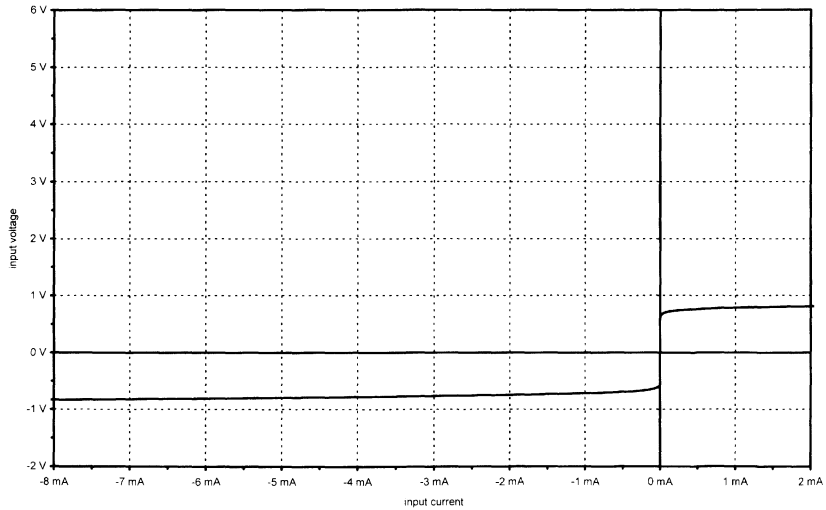

Figure 19: Input Characteristics of the SN74LV244 at V_{CC} = 0V

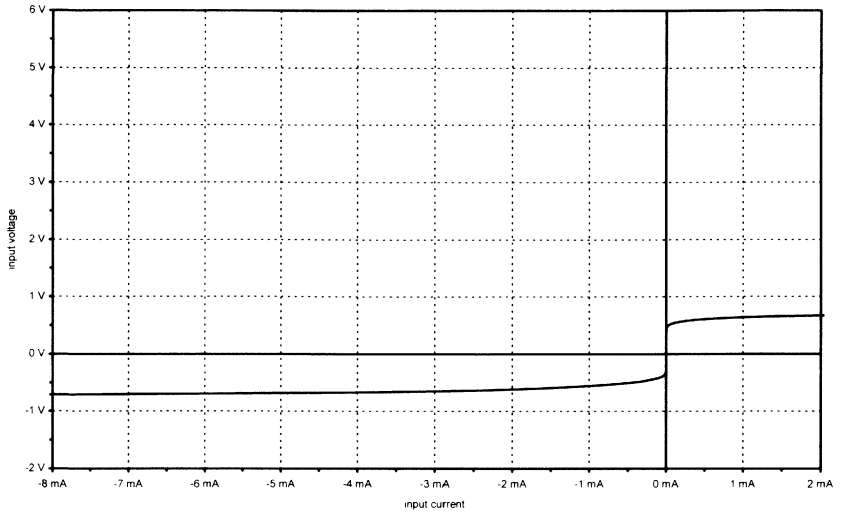

Figure 20: Output Characteristics of the SN74LV244 at V_{CC} = 0V

3.2.2 LVC without Supply voltage

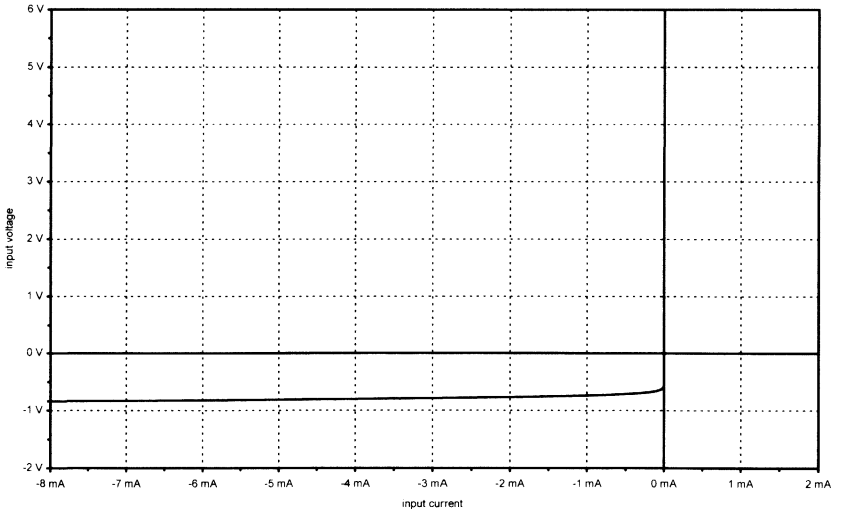

Figure 21: Input Characteristics of the SN74LVC244 at V_{CC} = 0V

As a result of the ESD protection circuitry used for the inputs without diode paths connected to V_{CC}, the inputs of the LVC circuits (in contrast to the LV circuits) are in a positive voltage range at a high impedance (Figure 21). The outputs however show a diode characteristic in a positive voltage range, and are therefore normally not suitable for systems which are partitially switched off (Figure 22).

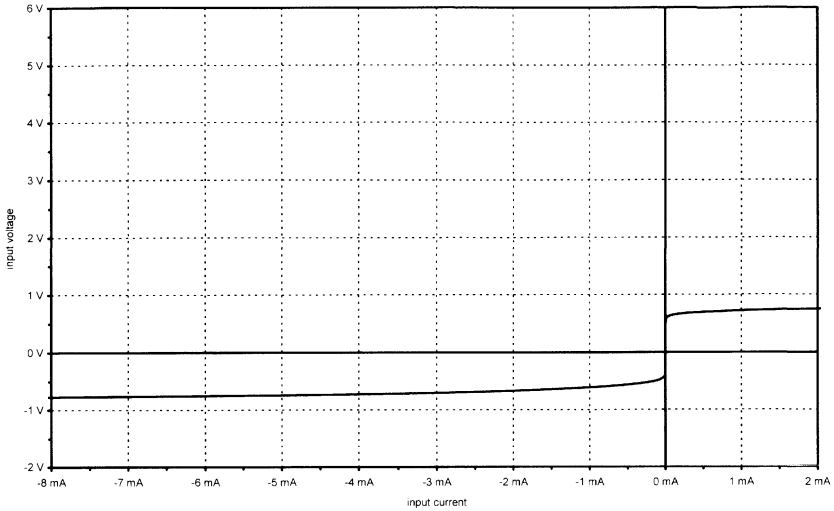

Figure 22: Output Characteristics of the SN74LVC244 at V_{CC} = 0V

3.2.3 ALVC without Supply Voltage

As a result of the diode paths to VCC and GND resulting from the ESD protection circuitry (Figure 8, Page 11), the ALVC family has the same behavior as the LV family. At a supply voltage of 0V it is not possible to apply a voltage of more than about 0.7V to the inputs or outputs without damaging the component as a result (Figures 23 and 24). ALVC circuits must therefore not be used in systems where the supply voltage is sometimes switched off.

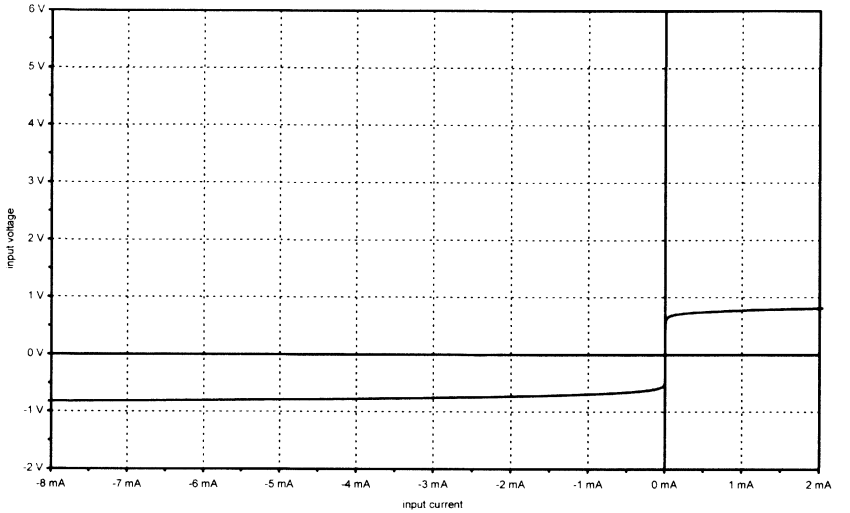

Figure 23: Input Characteristics of the SN74ALVC16244 at V_{CC} = 0V

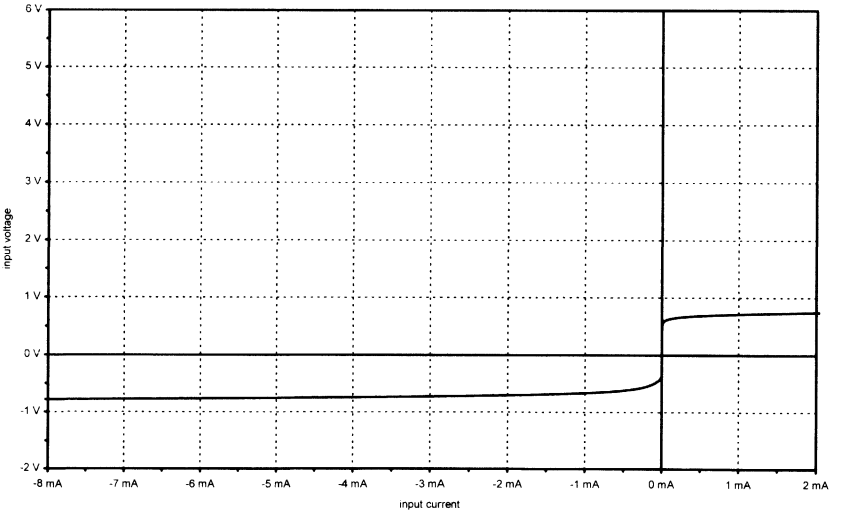

Figure 24: Output Characteristics of the SN74ALVC16244 at V_{CC} = 0V

3.2.4 LVT without Supply Voltage

As is typical with CMOS, the inputs with positive voltages are at a high impedance, since the ESD protection circuitry will also not be at a low impedance under these conditions (Figure 25). As a result of the bipolar output stage the outputs of LVT circuits will be at a high impedance, if the supply voltage is 0V (Figure 26). The LVTZ parts are provided with a Power-Up Tristate circuit, which puts the outputs in a high impedance state when V_{CC} goes under the value below which correct operation can no longer be maintained. A defined behavior of the component is therefore also assured during the period when the supply voltage is being switched on and off.

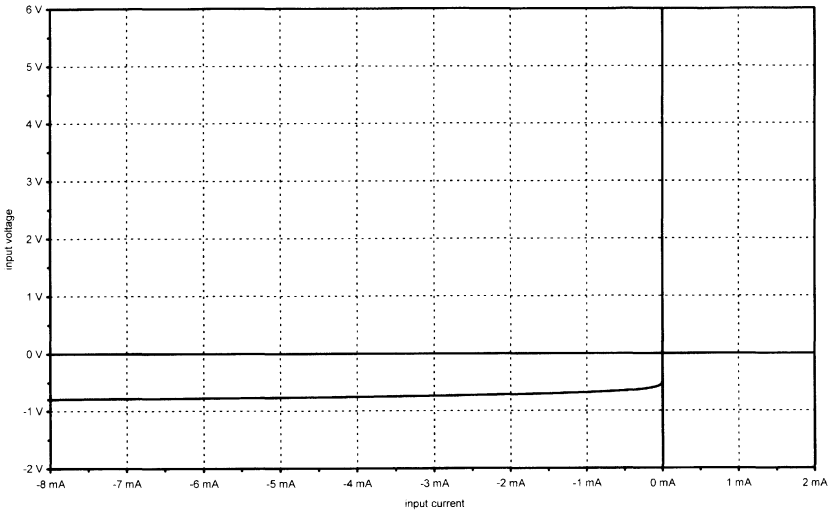

Figure 25: Input Characteristics of the SN74LVT244 at V_{CC} = 0V

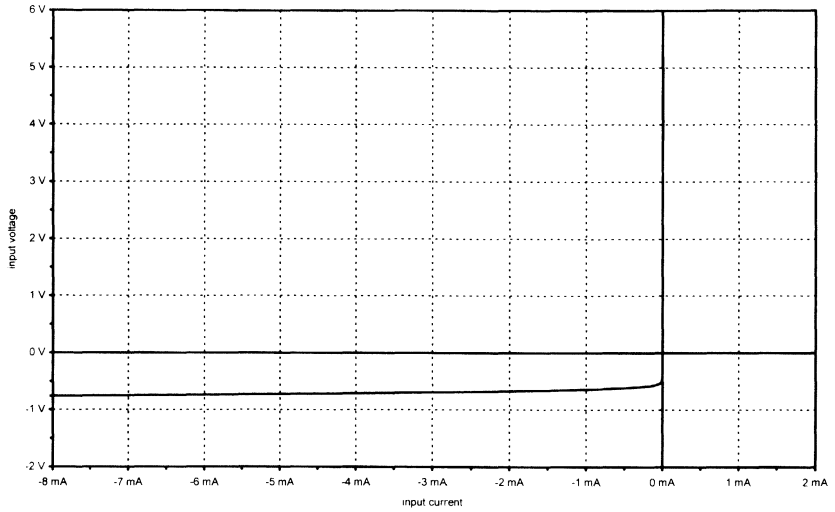

Figure 26: Output Characteristics of the SN74LVT244 at V_{CC} = 0V

3.3 Power Consumption

The power consumption of digital CMOS circuits increases linearly with increasing clock rates. This increase is much less significant with bipolar circuits. The LVT is a BiCMOS family, and therefore has both CMOS and bipolar elements, such that this family shows a mixed behavior.

3.3.1 Static Power Consumption

Table 5 uses the '244 as an example to show the static power consumption of the four families LV, LVC, ALVC and LVT. The typical current consumption of these components is considerably less.

The CMOS feature of an extremely low power consumption with static operation highlights the three representatives of the pure CMOS families: LV244, LVC244 and ALVC16244. Their supply current is a maximum of 500µA, corresponding to a maximum power consumption of 1.8mW. If the outputs are in a high impedance state, then their power consumption is reduced to a maximum of 72µW.

As a typical representative of a BiCMOS family, the 'LVT244 shows a significantly higher power consumption in static operation than the CMOS families. On the other hand, the maximum value of 12mW is still comparatively low. With high impedance outputs, the maximum power consumption is reduced to 190µW.

	Test Conditions		LV244	LVC244	ALVC16244	LVT244
I_{CC}	V_{CC} = 3.6V V_I = V_{CC} or GND I_O = 0	Outputs high	max. 20µA	max. 20µA	max. 40µA	max. 190µA
		Outputs low	max. 20µA	max. 20µA	max. 40µA	max. 12mA
		Outputs disabled	max. 20µA	max. 20µA	max. 40µA	max. 190µA
ΔI_{CC}	V_{CC} = 3.0V to 3.6V one input at V_{CC} - 0.6V other inputs at V_{CC} or GND		max. 500µA	max. 500µA	max. 500µA	max. 200µA

Table 5: Static power consumption of the 'LV244, 'LVC244, 'ALVC16244 and 'LVT244

Figure 27 shows a CMOS input stage, as used in CMOS and BiCMOS circuits. If the input voltage is the same as the supply voltage, then the P channel transistor is not conducting, and almost no current flows from V_{CC} to GND. It behaves in a similar way with an input voltage of 0V, whereby in this case the N channel transistor is not conducting. If the input voltage is not at the same potential as the supply voltage or GND, then the transistors of this input stage will operate in a linear region, and both transistors will be more or less conducting. As a result of this situation, the power consumption in static and dynamic operation increases, if the input level is not the same as the supply voltage or the GND potential. The parameter ΔI_{CC} in data books takes this fact into account. The corresponding typical characteristics are shown in Figures 28, 29, 30 and 31.

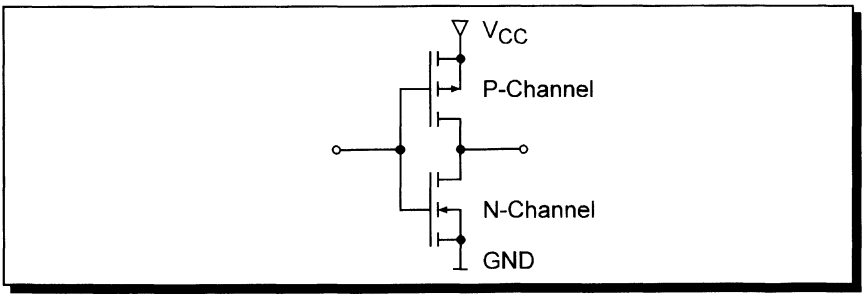

Figure 27: Circuit of a CMOS or BiCMOS input stage

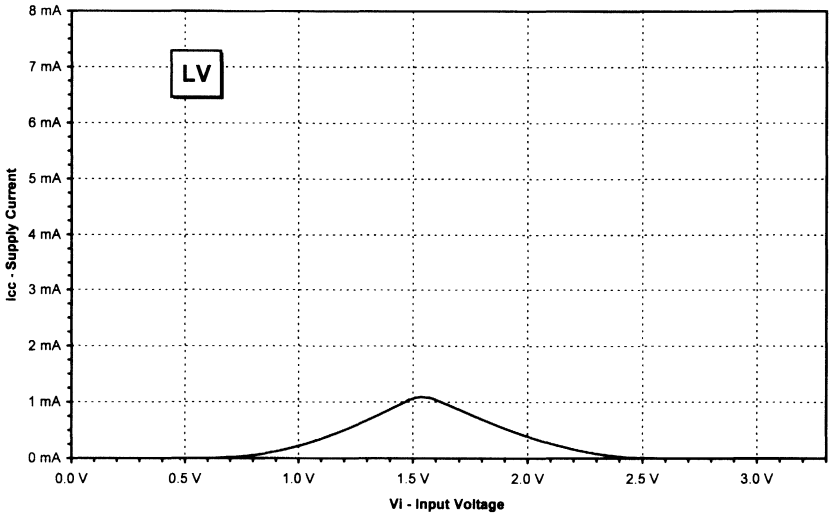

Figure 28: Current consumption of the LV as a function of the input voltage

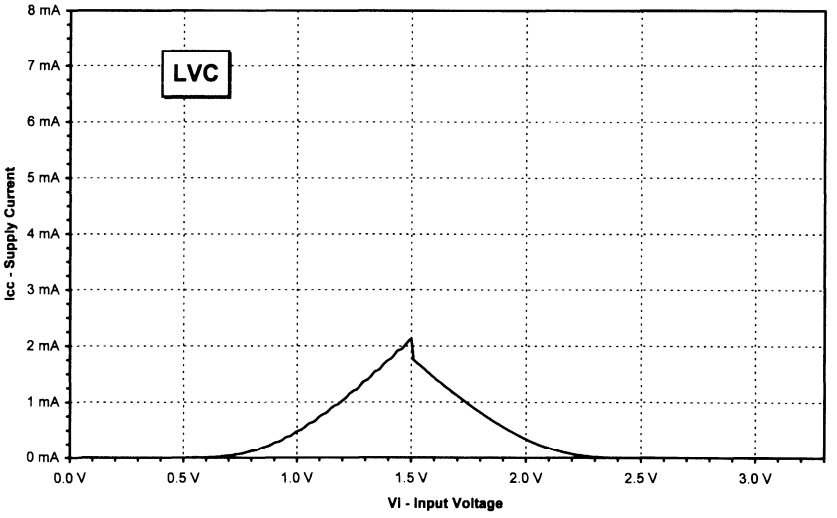

Figure 29: Current consumption of the LVC as a function of the input voltage

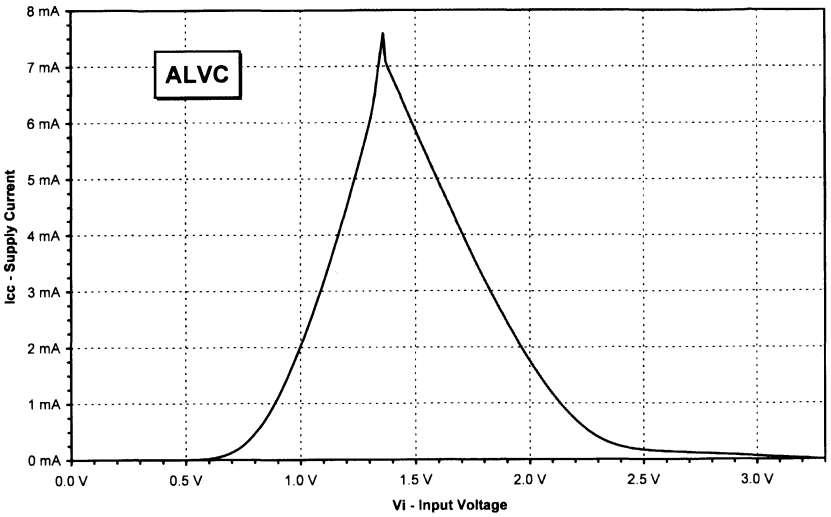

Figure 30: Current consumption of the ALVC as a function of the input voltage

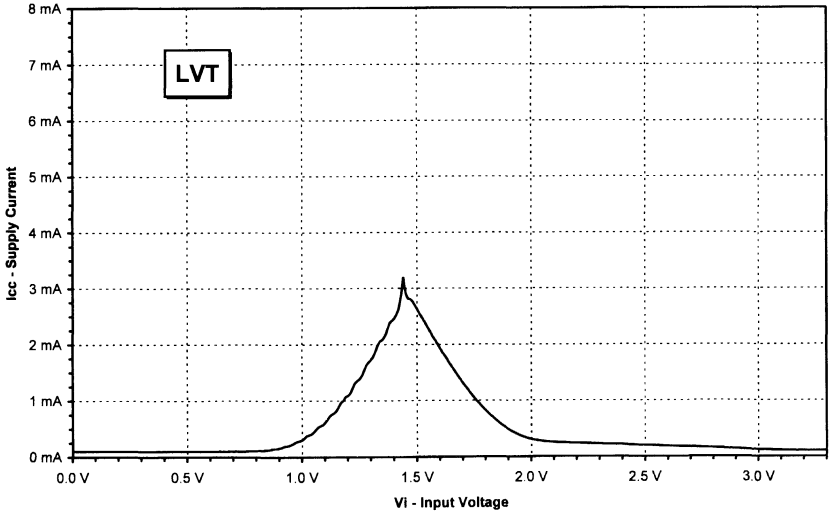

Figure 31: Current consumption of the LVT as a function of the input voltage

3.3.2 Dynamic Power Consumption

With all four logic families the power consumption increases with increasing operating frequency (Figure 32). This increase of the power consumption is partly the result of the fact that internal capacitances need to be continuously charged and discharged, and partly because current "spikes" are generated when the output transistors are switched on and off. In order to evaluate the power consumption of the bus driver alone, the curves in Figure 32 were measured without a load circuit on the outputs. A capacitive load on the output will further increase the dynamic power consumption

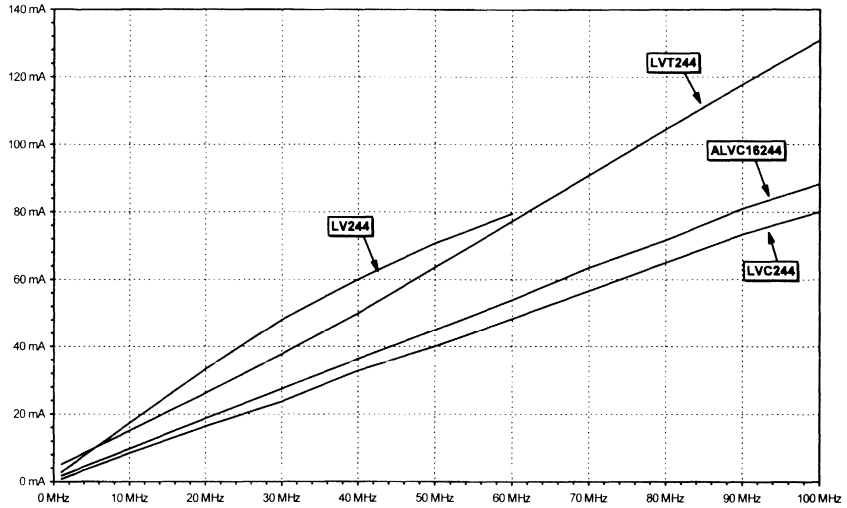

Figure 32: Power consumption without load on the outputs as a function of the frequency.

3.4 Dynamic Behavior

3.4.1 Switching Speed

If the maximum delay times guaranteed in data sheets are examined (Table 6), it will be seen that the circuits of the LV family are by far the slowest in this 3.3V family quartet. The typical values and the dependence of the delay time on the number of outputs being switched is shown in Figures 33 and 34. Since ALVC is only available in the Widebus™ package, the favorable characteristics of this package improve the results with this measurement. In Figures 33 and 34 the measurement results with a LVC16244 in the Widebus™ package have been included for comparison, whereby it can be seen that the LVC16244 behaves almost identically to the ALVC16244. It can clearly also be seen from this that the influence of the package has a more significant effect on the measurement results, than the electrical characteristics of the logic family in question.

	from	to	LV244	LVC244	ALVC16244	LVT244
t_{PLH}	A	Y	max. 19ns	max. 6.5ns	max. 3.6ns	max. 4.3ns
t_{PHL}	A	Y	max. 19ns	max. 6.5ns	max. 3.6ns	max. 4.2ns

Table 6: Delay times guaranteed in the data sheets of the LV244, LVC244, ALVC16244 and LVT244, at V_{CC} = 3.3V ± 0.3V and over a temperature range of -40°C to +85°C.

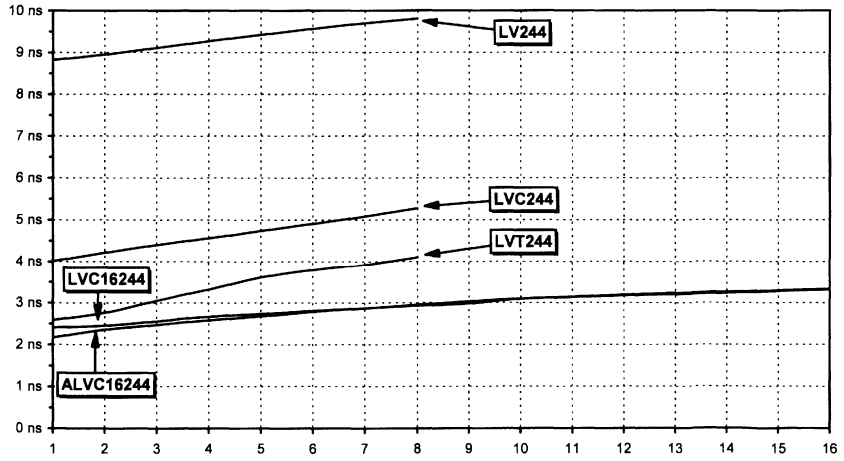

Figure 33: Delay Time t_{PLH} as a function of the number of outputs being switched

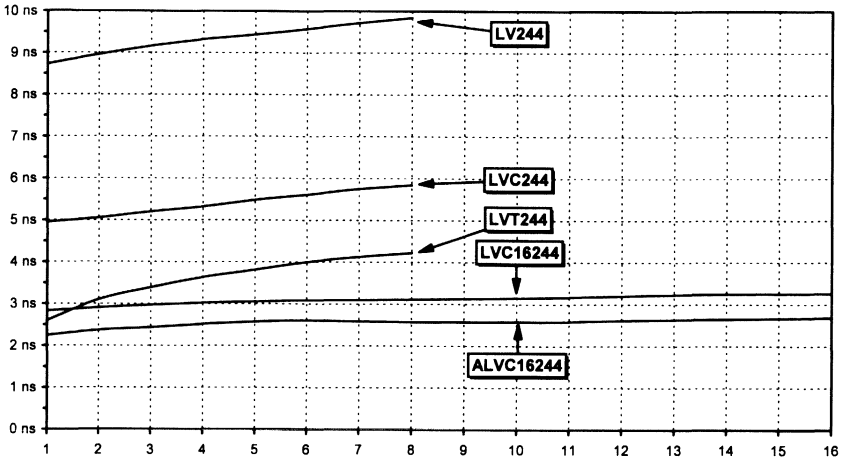

Figure 34: Delay time t_{PHL} as a function of the number of outputs being switched

3.4.2 Characteristic Curves

Figures 35 and 36 show typical characteristic curves of the four logic families LV, LVC, ALVC and LVT, using as an example the Bus Driver '244. The curves were measured at the outputs with a load of 500Ω and 50pF connected to GND in parallel. The different delay times and steepness of the edges can be clearly seen. The slowest family LV has a significantly longer rise and fall time than the two fastest families ALVC and LVT. As a result of the fast edges of the LVC, ALVC and LVT families, when designing circuit boards more attention must be paid to line reflections with these components than with the LV family.

	'LV244	'LVC244	'ALVC16244	'LVT244
Rise Time (10% - 90%)	7.2ns	3.1ns	2.5ns	2.3ns
Fall Time (90% - 10%)	4.8ns	2.9ns	2.2ns	1.8ns

Table 7: Typical Rise and Fall Times at V_{CC}=3.3V and 25°C.

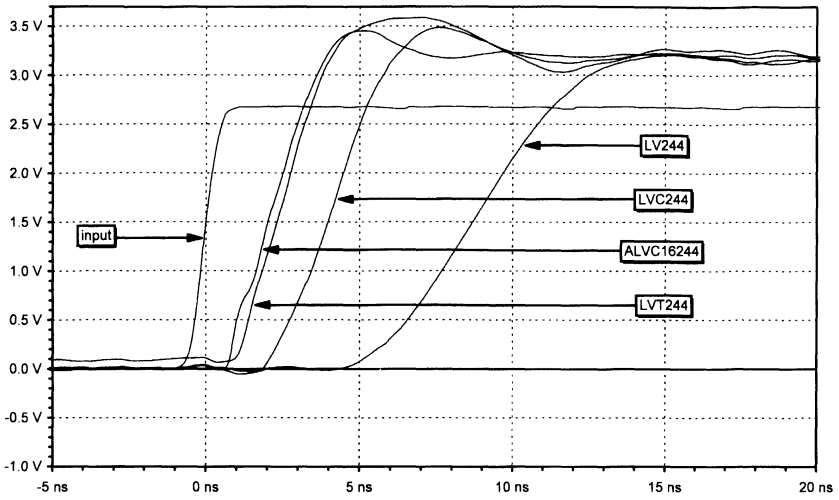

Figure 35: Rising edges of the four components 'LVC244, 'ALVC16244 and 'LVT244, with a load of 500Ω and 50pF connected to GND.

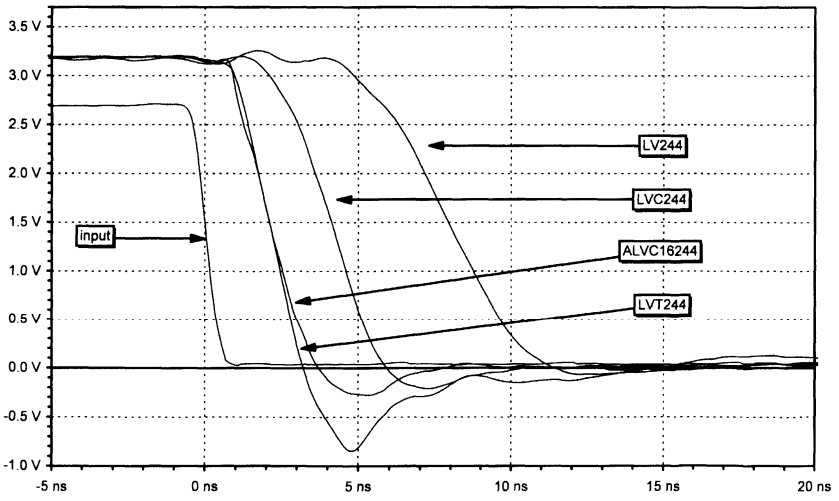

Figure 36: Falling edges of the four circuits 'LV244, 'LVC244, 'ALVC16244 and 'LVT244, with a load of 500Ω and 50pF connected to GND.

4. Summary

If low power consumption or high switching speed are required in a system, then the supply voltage must inevitably be reduced. Conventional CMOS logic families such as HC and AC allow operation at very low supply voltages; however, this reduces the performance of these circuits considerably. Specially designed for operation at 3.3V, the logic families LV, LVC, ALVC and LVT feature the performance characteristics of the 5V families when operated at only 3.3V supply voltage. In order to provide the most suitable circuit for every application, TEXAS INSTRUMENTS offers the following four logic families:

LV, which at 3.3V has the characteristics of the 5V family HCMOS.

LVC and ALVC, corresponding to the 5V family AC, whereby the ALVC circuits are significantly faster than the LVC.

LVT, which as a BiCMOS family provides the characteristics of the ABT, but with TTL compatible input and output levels.

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